Chapter 4 : INTERRUPTS.

SECTION-II (SHORT QUESTIONS)

1. Define partial address decoding. Define the term interrupt.

Partial address decoding:
A decoding method where **only some higher-order address lines** are used to generate a chip-select signal, causing the device to appear at **multiple memory locations (mirrored addresses)**.

Interrupt:
A hardware or software signal that **pauses the current program** so the processor can execute a specific service routine.

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2. Define absolute address decoding. What is an interrupt vector?

Absolute address decoding:
A method where **all address lines** are used to uniquely select a device, ensuring the device responds to **only one specific address range**.
Interrupt vector:
A specific **memory address containing the starting location** of an Interrupt Service Routine (ISR).

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3. Define hardware interrupt.

A hardware-generated signal that forces the CPU to temporarily stop its ongoing task and execute a service routine.
Source: Intel 8086 User’s Manual

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4. Define maskable interrupt.

A hardware interrupt that can be **enabled or disabled (masked)** using the CPU's interrupt flag (IF).
Source: Intel Architecture Software Developer Manual

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5. Define non-maskable interrupt.

A high-priority hardware interrupt that **cannot be disabled**, usually used for critical events.
Source: Intel 8086 Documentation

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6. Function of signals INTR and INTĀ.

- **INTR (Interrupt Request):** A maskable interrupt request from hardware.
- **INTĀ (Interrupt Acknowledge):** Signal from CPU indicating it has accepted the interrupt request.
  Source: Intel 8086 Hardware Reference

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7. Define software interrupt.

An interrupt triggered by an **instruction (INT n)** rather than hardware.
Source: Intel Software Developer Manual

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8. List five interrupt instructions for microprocessor.

1. **INT n**
2. **INT 3**
3. **INTO**
4. **IRET / IRETD**
5. **INT 0 (Divide Error)**
   Source: Intel SDM

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9. Function of INTO instruction?

Executes an interrupt (**Type 4 Overflow Interrupt**) **only if the OF (Overflow Flag) = 1**.
Source: Intel Instruction Set Reference

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10. Function of INT3 instruction?

Generates a **breakpoint interrupt (Type 3)** used for debugging.
Source: Intel SDM Vol. 2

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11. Define error interrupt.

An interrupt generated when the processor detects **an error condition**, such as divide-by-zero or overflow.
Source: Intel 8086 Vector Table Specification

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12. Programmable Interrupt Controller (PIC).

A device (like **Intel 8259**) that manages hardware interrupts and sends them to the CPU based on **priority and masking rules**.
Source: Intel 8259A Datasheet

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13. What is meant by Interrupt Structure?

The organization of **hardware, vector table, priority levels, and signal handling mechanisms** used to process interrupts.
Source: Intel Architecture Manuals

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14. Hardware interrupts of 8086.

1. **NMI (Non-maskable interrupt)**
2. **INTR (Maskable interrupt request)**
   Source: Intel 8086 Manual

15. How many software interrupts are available for 8086?

256 software interrupts (Type 0 to Type 255).
Source: Intel 8086 Interrupt Vector Table

SECTION-III (LONG QUESTIONS)

1. Define interrupt and describe software & hardware interrupts.

(Full long answer with citations included)

An interrupt is a mechanism that **temporarily halts normal execution** so a special routine (ISR) can run.

Hardware Interrupts

- Generated by external devices.
- Types: **INTR, NMI**.
- NMI is unmaskable; INTR is maskable.
  Source: Intel 8086 User’s Manual

Software Interrupts

- Generated by **INT n** instruction.
- Used for OS calls, debugging, BIOS services.
  Source: Intel SDM

2. Steps when microprocessor receives an interrupt signal.

1. Completes current instruction
2. Pushes **FLAGS** register
3. Clears IF and TF
4. Pushes **CS:IP**
5. Loads new CS:IP from interrupt vector table
6. Executes ISR
7. Returns using IRET
   Source: Intel 8086 Manual

3. Operation of 8259 Programmable Interrupt Controller.

Key points:

- Receives up to **8 hardware interrupts**
- Prioritizes them
- Sends interrupt to CPU via INTR
- CPU responds with INTĀ
- 8259 outputs interrupt vector type
- Supports modes: Fully nested, rotating, special mask, polling
  Source: Intel 8259A Datasheet**