Chapter 3 MEMORY AND BASIC I/O INTERFACE

SECTION-II — SHORT QUESTIONS

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1. Define partial address decoding.

Partial address decoding uses only some higher-order address lines to generate a chip-select signal. Lower lines are treated as “don’t care,” reducing hardware cost but allowing multiple addresses to point to the same device (address aliasing).

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2. Define absolute address decoding.

Absolute decoding uses *all* valid address lines to uniquely identify a memory or I/O device. This ensures each location has a single, exact address with no aliasing.

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3. Name two microprocessors with an 8-bit memory interface.

Examples include the **Intel 8085** and **Zilog Z80**, both widely used 8-bit microprocessors with an 8-bit data bus.
Sources:
8085
Z80

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4. Function of the BHE¯\overline{BHE}BHE signal in a 16-bit interface.

BHE¯\overline{BHE}BHE (Bus High Enable) selects the upper 8 bits of a 16-bit data bus during memory read/write operations. It enables access to the high byte when needed.

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5. Define handshaking.

Handshaking is a control-signal method where two devices coordinate data transfer using signals like READY or ACK. It ensures synchronized communication between CPU and I/O devices.

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6. Define memory-mapped I/O decoding.

In memory-mapped I/O, I/O devices share the same address space as memory. CPU accesses them using regular memory instructions such as MOV or LOAD.

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7. Define isolated I/O decoding.

Isolated or port-mapped I/O uses a separate address space for peripherals. CPU accesses ports using special instructions such as IN and OUT.

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8. Define programmable interval timer.

A programmable interval timer (like Intel 8254) generates accurate timing delays by counting clock pulses. It can operate in multiple modes such as periodic, one-shot, or square wave.

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9. What is meant by UART?

UART (Universal Asynchronous Receiver-Transmitter) converts parallel data into serial form and vice versa for asynchronous communication.

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10. Difference between half-duplex and full-duplex transmission.

Half-duplex allows data to move in both directions but not at the same time (e.g., walkie-talkies). Full-duplex allows simultaneous two-way communication (e.g., telephone).

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11. Purpose of a programmable communication interface.

It controls serial communication parameters—baud rate, parity, stop bits—allowing devices with different communication settings to connect properly.

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12. Disadvantages of mechanical switch keyboards.

Mechanical keyboards are noisy, consume more power, and their moving parts can wear out over time. They are also costlier than membrane-based designs.

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13. Merits of capacitive keyboards.

Capacitive keyboards are durable, quiet, fast, and have no mechanical contacts to wear out. They provide smooth, reliable keystrokes with longer lifespan.

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14. Formula for voltage step in an 8-bit DAC.

Step Size=Vref28−1=Vref255\text{Step Size} = \frac{V_{ref}}{2^8 - 1} = \frac{V_{ref}}{255}Step Size=28−1Vref=255Vref

This gives the smallest analog change per digital increment.

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15. Difference between sector and track.

A **track** is a circular path on a disk platter. A **sector** is a subdivision of a track, representing the smallest addressable storage unit.

16. Define pointer. Name any two pointers.

A pointer stores the memory address of another variable or location. Examples include **Stack Pointer (SP)** and **Program Counter (PC)**.

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17. Define Digitizer.

A digitizer converts analog input—such as handwriting or graphics—into digital form for computer processing.

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18. Function of a scanner.

A scanner reads physical documents or images and converts them into digital pixel data for storage, editing, or printing.

SECTION-III — LONG QUESTIONS

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1. Explain Input Interface with diagram.

An input interface is the electronic circuitry that allows an input device to communicate with the CPU. It typically includes a data register, status register, and control logic. The status register indicates conditions such as “data available” or “device ready.” When a device generates new data, it sets status bits and may trigger an interrupt. The CPU then reads the data register using a read instruction. Handshaking signals ensure synchronization between the device and CPU. Examples of input interfaces include the keyboard controller and UART input module.

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2. Draw block diagram of DAC and explain its working.

A Digital-to-Analog Converter contains an input latch, a resistor network (often R-2R ladder), a reference voltage source, and an output amplifier. The digital input is first stored in the latch. The resistor network converts weighted binary bits into proportional analog voltages or currents. The reference voltage defines the maximum output level. The output amplifier conditions the signal to produce a stable analog output. Higher digital values correspond to higher analog output levels. An 8-bit DAC divides the reference voltage into 256 steps.

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3. Discuss construction and working of a keyboard.

A keyboard is constructed using a matrix of rows and columns, where each key connects a specific row and column. A keyboard controller continually scans this matrix using a technique called “row-column scanning.” When a key is pressed, it closes a specific row–column connection that the controller detects. The controller then generates a **scan code** representing that key. Debouncing circuitry ensures that key noise does not generate repeated characters. The scan code is transferred to the CPU via an input interface or interrupt.

4. Discuss construction and working of a Video Display Unit (VDU).

A VDU consists of display hardware (LCD/LED panel), video controller, and video memory (VRAM). The CPU writes pixel or character data into VRAM. The video controller continuously reads this memory and converts it into timing signals required for the display. In CRTs, electron beams draw pixels line by line; in LCDs, transistors control the brightness of individual pixels. Refresh cycles ensure the screen maintains a stable image. The VDU operates independently once VRAM is updated.

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5. Explain different modes of the 8254 Programmable Interval Timer.

The Intel 8254 includes three programmable counters operating in six modes. **Mode 0** generates an interrupt at terminal count. **Mode 1** produces a one-shot pulse. **Mode 2** acts as a rate generator for periodic interrupts. **Mode 3** generates a square wave output. **Mode 4** produces a software-triggered strobe pulse. **Mode 5** gives a hardware-triggered strobe. These modes are used for clocks, event counting, and waveform generation.

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6. Explain linear address decoding with diagram.

Linear (partial) decoding uses only selected high-order address lines to activate a memory or I/O device. Lower lines are ignored, simplifying hardware and reducing decoder cost. However, ignoring bits causes **address aliasing**, meaning the same device appears at multiple addresses. A decoder (such as 3-to-8) generates chip-select signals from high-order bits. This technique is used in small systems where cost and layout simplicity matter more than perfect address uniqueness.